WHAT IS CLAIMED IS:

1.   A system for interleaving data in a communications device, wherein the data is comprised of a plurality of data blocks, each block having a plurality of symbols, the system comprising:

a memory segmented into a plurality of addressable memory blocks, each memory block having a unique address;

a write module coupled to the memory, the write module configured to write symbols to the addressable memory blocks;

a read module coupled to the memory, the read module configured to read symbols from the addressable memory blocks in an interleaved fashion;

means for determining an interleaving sequence for transmitting symbols of a stored data block wherein the interleaving sequence includes a sequence of memory addresses; and

means for sequentially communicating each memory address in the interleaving sequence to the read module first and then to the write module;

wherein said read module is further configured to receive the memory address and to read the symbol stored in the memory address; and

wherein said write module is further configured to receive the memory address and to write a symbol from a next block of data to the memory address.

2.   The system of claim 1 wherein each memory address in the interleaving sequence is determined using an offset value wherein the offset value is calculated using the dimensions of the interleaver.

3.   The system of claim 1 wherein each memory address in the interleaving sequence is determined using a mapping function wherein the mapping function is calculated using the dimensions of the interleaver.

4.   The system of claim 1 further comprising a control module coupled to the determining means.

5.   The system of claim 1 further comprising a preprocessor coupled to the write module.

6. A method for interleaving data in a communications device including a block interleaver, wherein the data comprises a plurality of data blocks, each data block having a plurality of symbols, the method comprising the steps of:

(a) writing symbols from a first data block into an addressable memory according to an initial sequence of memory addresses;

(b) determining dimensions of the block interleaver for a current iteration;

(c) determining a memory address for a current position in an interleaving sequence wherein the number of positions in the sequence is equal to the size of a stored data block;

(d) reading the symbol stored in the determined memory address;

(e) writing a symbol from a next data block in the determined memory address;

(f) repeating steps (d) through (f) until all symbols of a stored data block have been read from memory; and

(g) repeating steps (b) through (g) until all data blocks have been transmitted by the communication device.

7. The method of claim 6 wherein the step of determining a memory address for a current position in the interleaving sequence further comprises the steps of:

(a) determining an offset value for the interleaving sequence, wherein the offset value is computed as $O_n = N \times O_{n-1}$ **mod***$(S-1)$ wherein the variable N is a width of the block interleaver, S is a size of the block interleaver and O_{n-1} is an offset of an immediately previous iteration; and

(b) determining a memory address to access, wherein the memory address is computed as $I_{n,m} = m \times O_n$ **mod***$(S-1)$ wherein the variable m is the position in the interleaved data sequence for which a symbol is to be read.

8.	The method of claim 6 wherein the communications device further includes a preprocessor.

9.	The method of claim 6 wherein the communications device further includes a control module.

10.	The method of claim 9 further comprising the step of:

(a)	receiving block interleaver configuration information to be used in determining the current interleaving sequence from the control module.

11.	A system for de-interleaving data in a communications device, wherein the data is comprised of a plurality of data blocks, each block having a plurality of interleaved data symbols, the system comprising:

a receiving block interleaver configured to have a width equal to the depth of a block interleaver which generated the plurality of interleaved symbols, the receiving block interleaver comprising:

a memory segmented into a plurality of memory blocks, each memory block having a unique address;

a write module coupled to the memory, the write module configured to write symbols to the addressable memory blocks;

a read module coupled to the memory; the read module configured to read symbols from the addressable memory blocks in a de-interleaved fashion;

means for determining an interleaving sequence for transmitting symbols of a stored data block wherein the interleaving sequence includes a sequence of memory addresses; and

means for sequentially communicating each memory address in the interleaving sequence to the read module first and then to the write module;

wherein said read module is further configured to receive the memory address and to read the symbol stored in the memory address; and

wherein said write module is further configured to receive the memory address and to write a symbol from a next block of data to the memory address.

12. The system of claim 11 wherein each memory address in the interleaving sequence is determined using an offset value wherein the offset value is calculated using the dimensions of the interleaver.

13. The system of claim 11 wherein each memory address in the interleaving sequence is determined using a mapping function wherein the mapping function is calculated using the dimensions of the interleaver.

14. The system of claim 11 further comprising a control module coupled to the determining means.

15. The system of claim 11 further comprising a preprocessor coupled to the write module.

16. A method for de-interleaving a block of interleaved data symbols in a receiving communications device including a block de-interleaver, wherein the data is received from a transmitting communications device having a block interleaver which generated the interleaved data sequence and wherein the block de-interleaver includes a receiving block interleaver having a width equal to a depth of the generating block interleaver, the method comprising the steps of:

(a) writing symbols from a first sequence of interleaved symbols into an addressable memory according to an initial sequence of memory address accesses;

(b) determining dimensions of the receiving block interleaver for a current iteration;

(c) determining a memory address for a current position in an interleaving sequence wherein the number of positions in the sequence is equal to the size of a stored data block;

(d) reading the symbol stored in the determined memory address;

(e) writing a symbol from a next data block in the determined memory address;

(f) repeating steps (d) through (f) until all symbols of a stored interleaved data block have been read from memory; and

(g)   repeating steps (b) through (g) until all received data blocks have been de-interleaved by the communication device.

17.   The method of claim 16 wherein the step of determining a memory address for a current position in the interleaving sequence further comprises the steps of:

(a)   determining an offset value for the interleaving sequence, wherein the offset value is computed as $O_n = N \times O_{n-1}$ **mod***(S-1) wherein the variable N is a width of the receiving block interleaver, S is a size of the receiving block interleaver and O_{n-1} is an offset of an immediately previous iteration; and

(b)   determining a memory address to access, wherein the memory address is computed as $I_{n,m} = m \times O_n$ **mod***(S-1) wherein the variable m is the position in the interleaved data sequence for which a symbol is to be read.

18.   The method of claim 16 wherein the receiving communications device further includes a preprocessor.

19.   The method of claim 16 wherein the receiving communications device further includes a control module.

20.   The method of claim 19 further comprising the step of:

(a)   receiving configuration information for the receiving block interleaver to be used in determining the current interleaving sequence from the control module.